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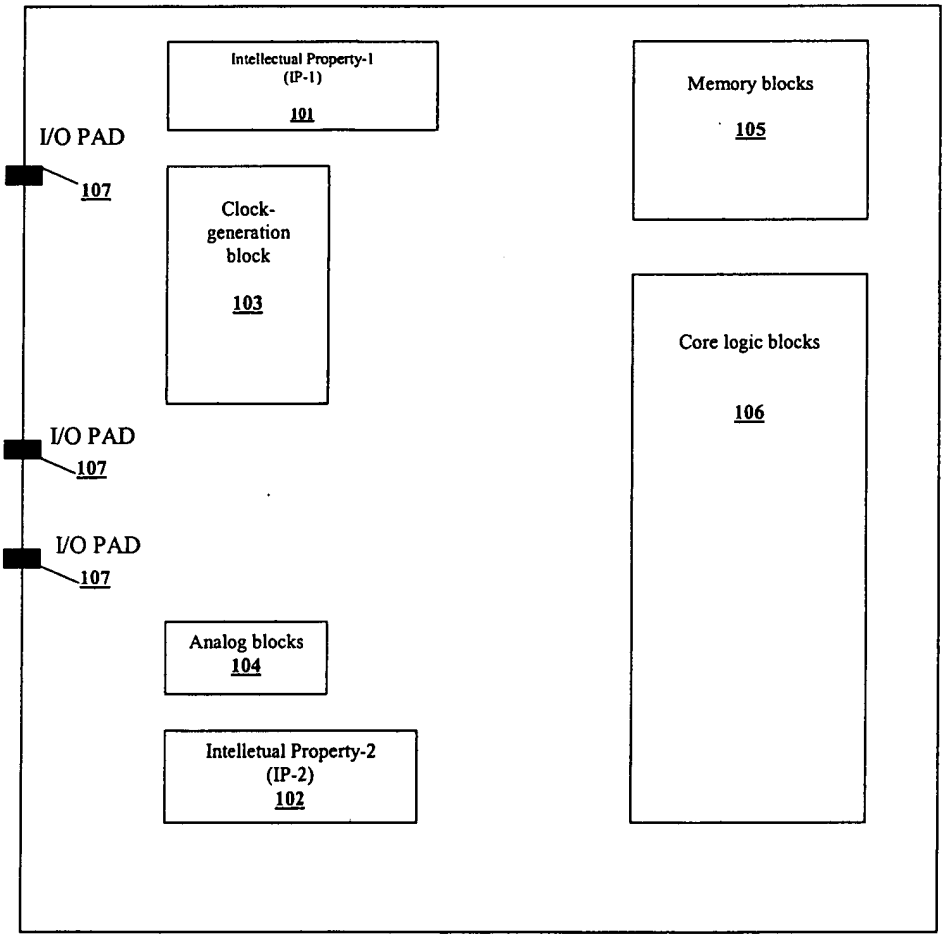

Intellectual Property-1
(IP-1)
101
Memory blocks
105
I/O PAD
107
Clock-
generation
block
103
Core logic blocks
106
I/O PAD
107
I/O PAD
107
Analog blocks
104
Intelletual Property-2
(IP-2)
102

FIGURE 1

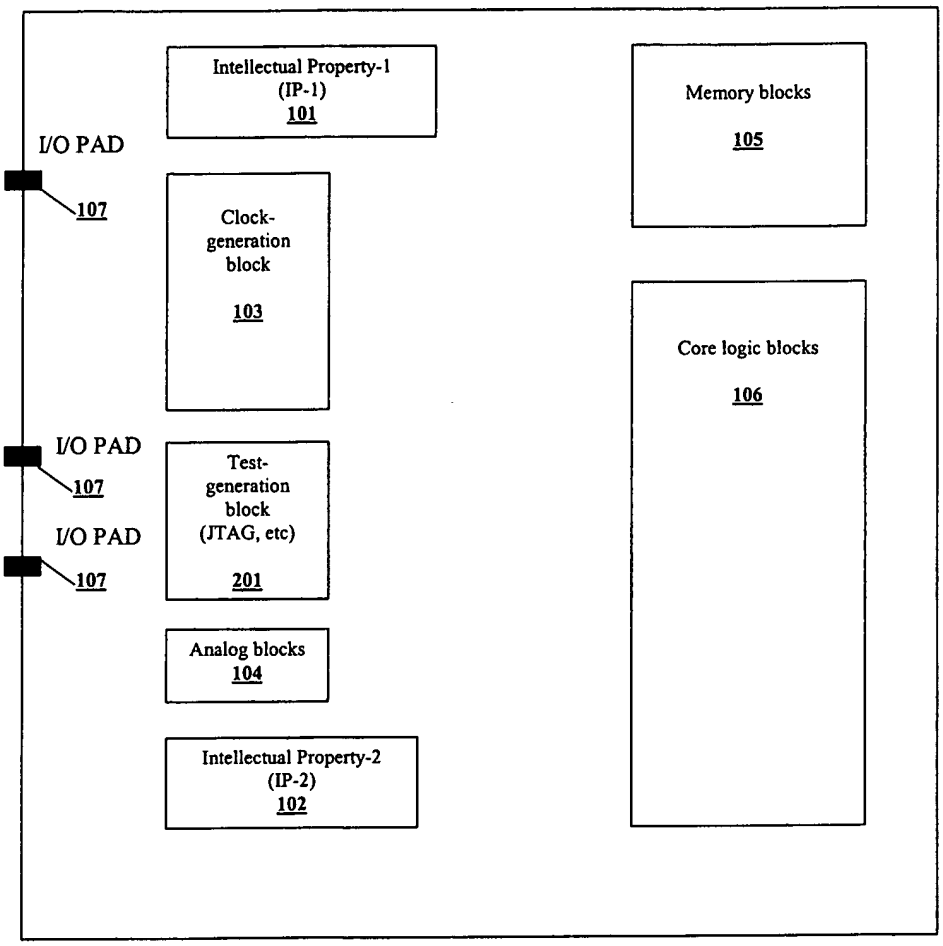

Intellectual Property-1
(IP-1)
101
Memory blocks
105
I/O PAD
107
Clock-
generation
block
103
Core logic blocks
106
I/O PAD
107
Test-
generation
block
(JTAG, etc)
201
I/O PAD
107
Analog blocks
104
Intellectual Property-2
(IP-2)
102

FIGURE 2

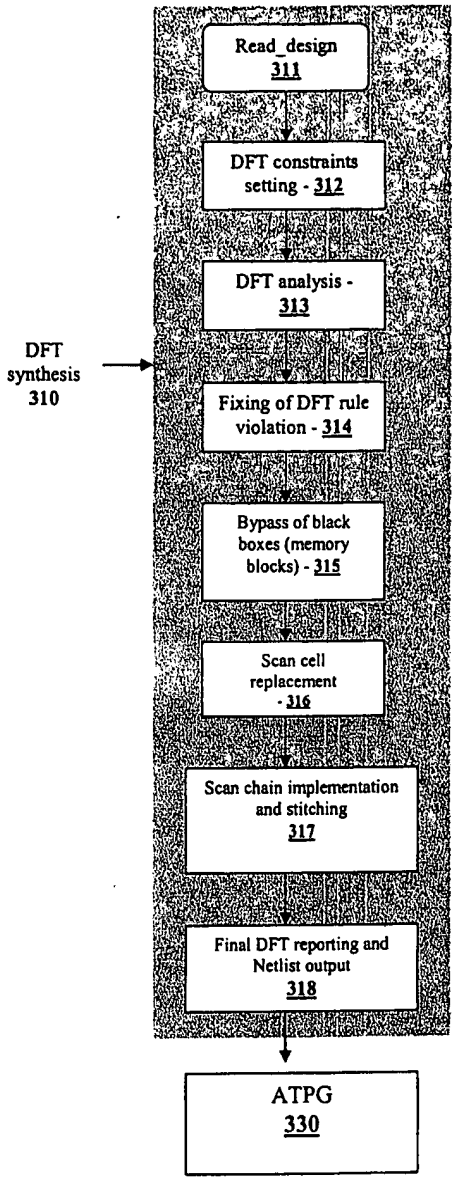


Figure 3B

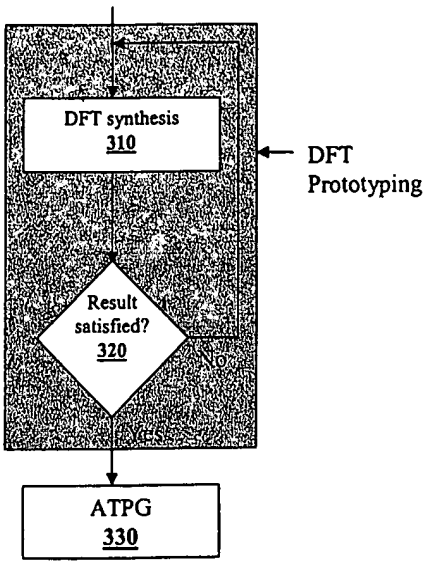
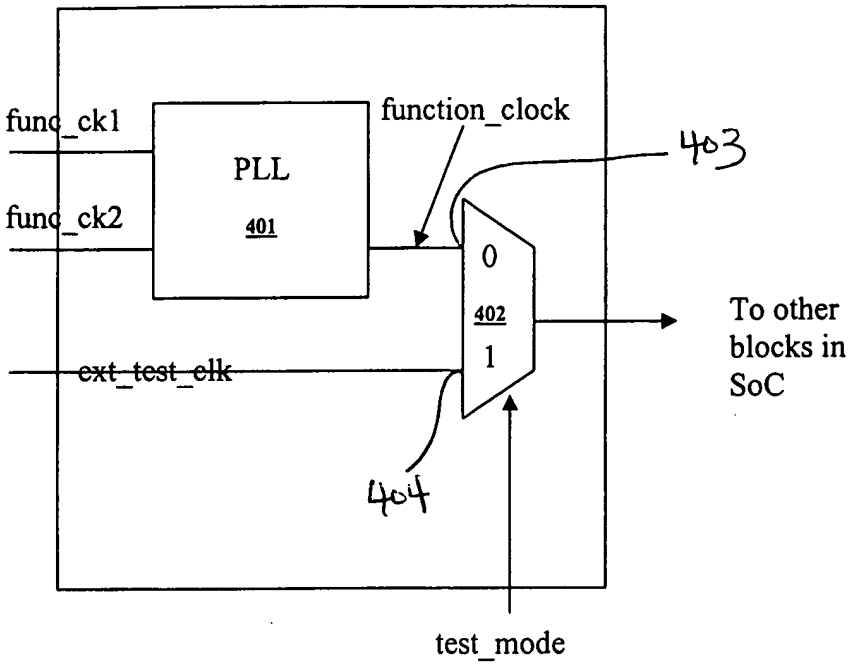
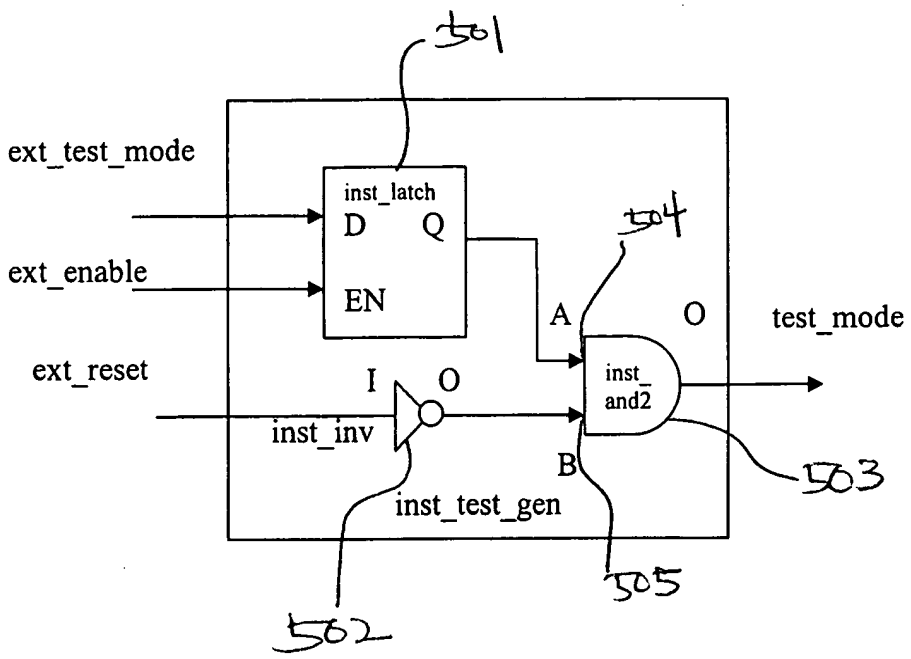


Figure 3A


func_ck1
func_ck2
PLL
401
function_clock
403
0
402
1
To other blocks in SoC
ext_test_clk
404
test_mode

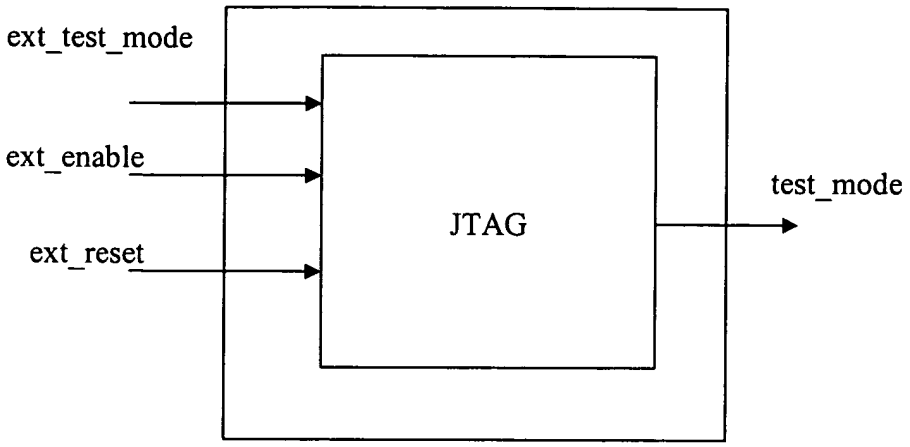
400

Figure 4


501
ext_test_mode
inst_latch
D
Q
EN
ext_enable
504
A
O
test_mode
ext_reset
I
O
inst_
and2
inst_inv
503
B
inst_test_gen
505
502

500

Figure 5



600

FIGURE 6

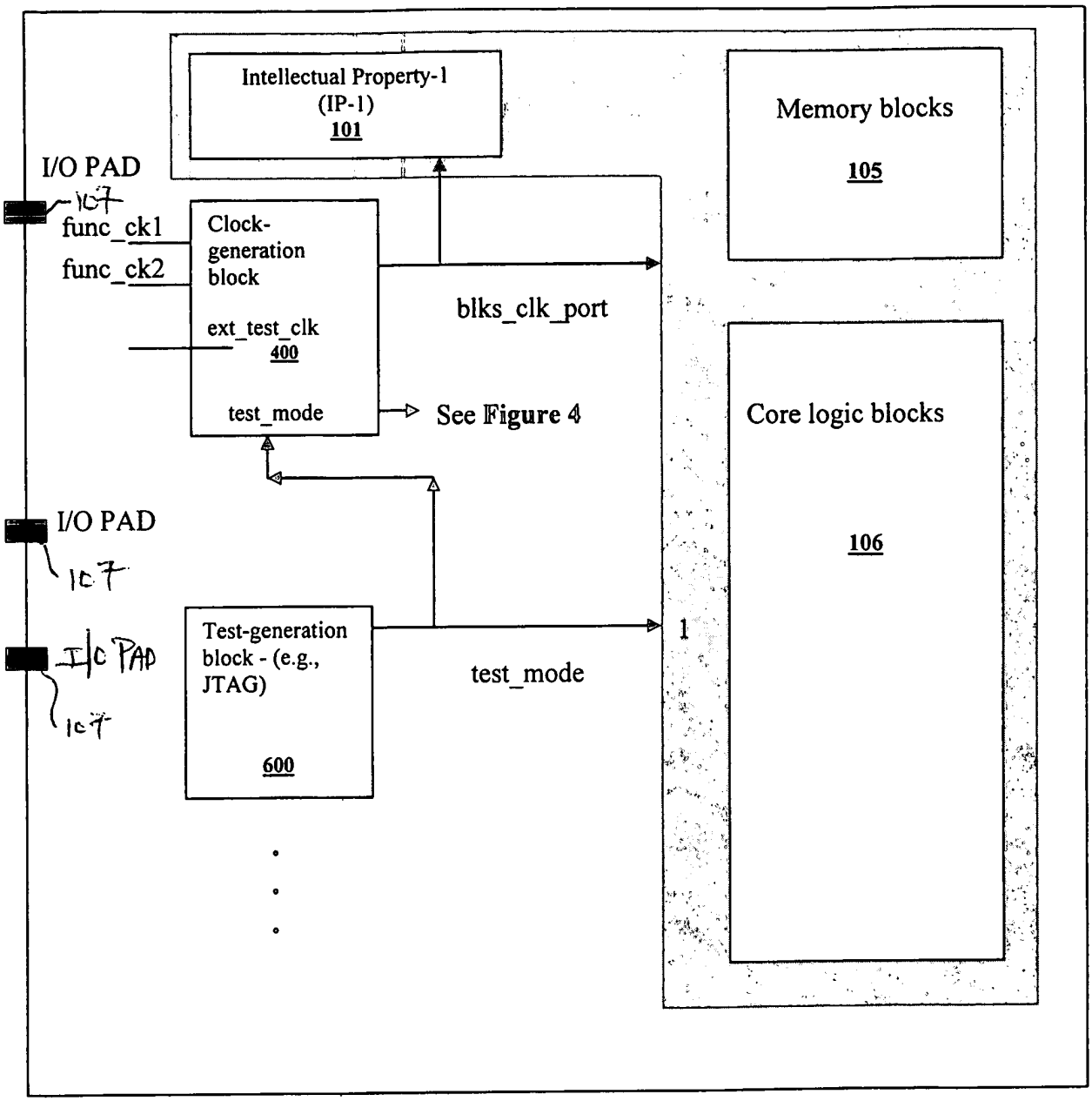

Intellectual Property-1
(IP-1)
101
Memory blocks
105
I/O PAD
107
func_ck1
func_ck2
Clock-generation block
ext_test_clk
400
test_mode
See Figure 4
blks_clk_port
Core logic blocks
106
I/O PAD
107
I/O PAD
107
Test-generation block - (e.g., JTAG)
600
test_mode

FIGURE 7

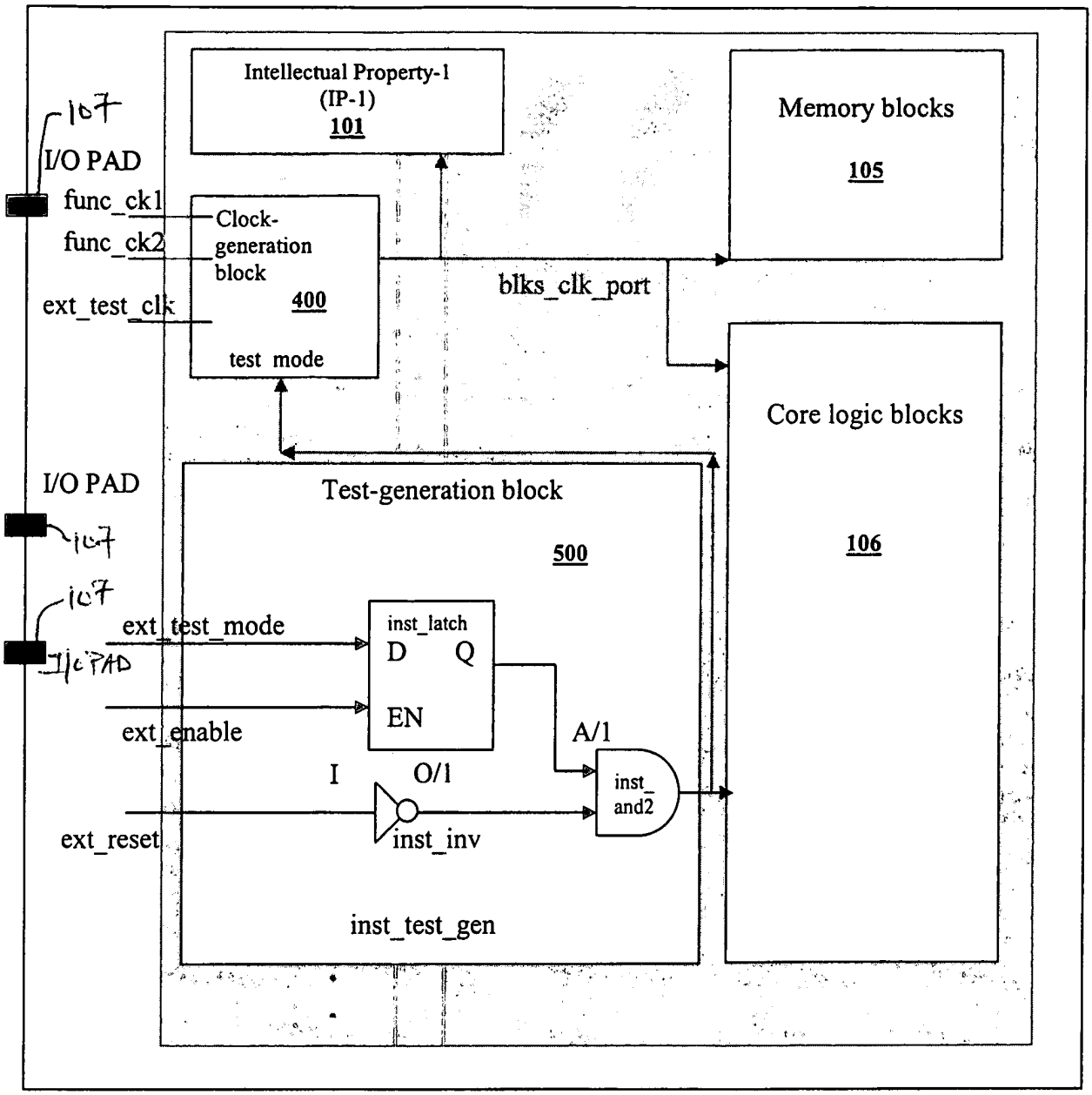

Intellectual Property-1
(IP-1)
101
Memory blocks
105
107
I/O PAD
func_ck1
func_ck2
ext_test_clk
Clock-generation block
400
test_mode
blks_clk_port
Core logic blocks
106
I/O PAD
107
107
I/O PAD
Test-generation block
500
ext_test_mode
inst_latch
D
Q
EN
ext_enable
A/1
I
O/1
inst_and2
ext_reset
inst_inv
inst_test_gen

FIGURE 8

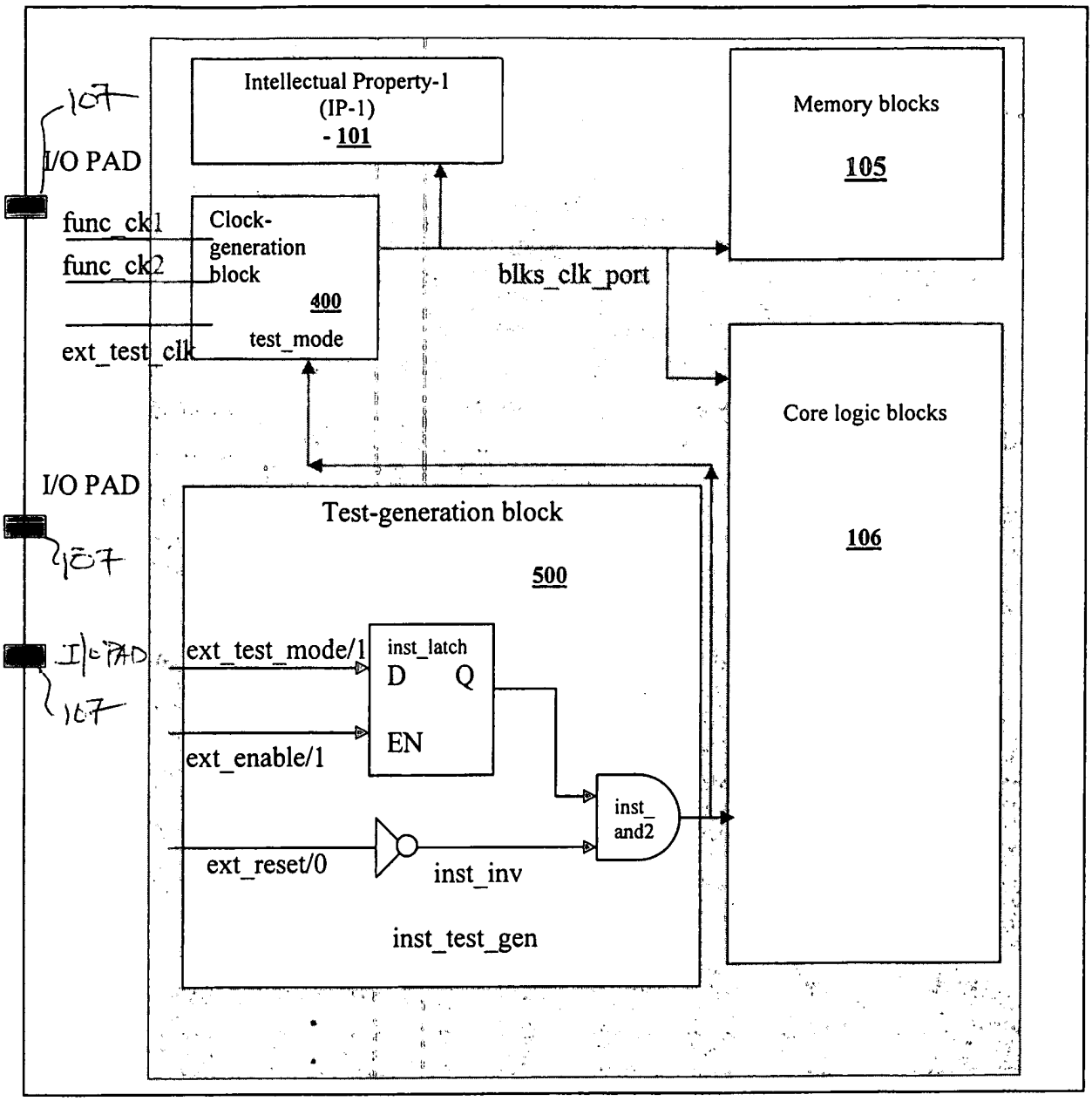

Intellectual Property-1
(IP-1)
- 101
Memory blocks
105
I/O PAD
func_ck1
func_ck2
ext_test_clk
Clock-generation block
400
test_mode
blks_clk_port
Core logic blocks
106
I/O PAD
Test-generation block
500
ext_test_mode/1
inst_latch
D
Q
EN
ext_enable/1
inst_and2
ext_reset/0
inst_inv
inst_test_gen

FIGURE 9

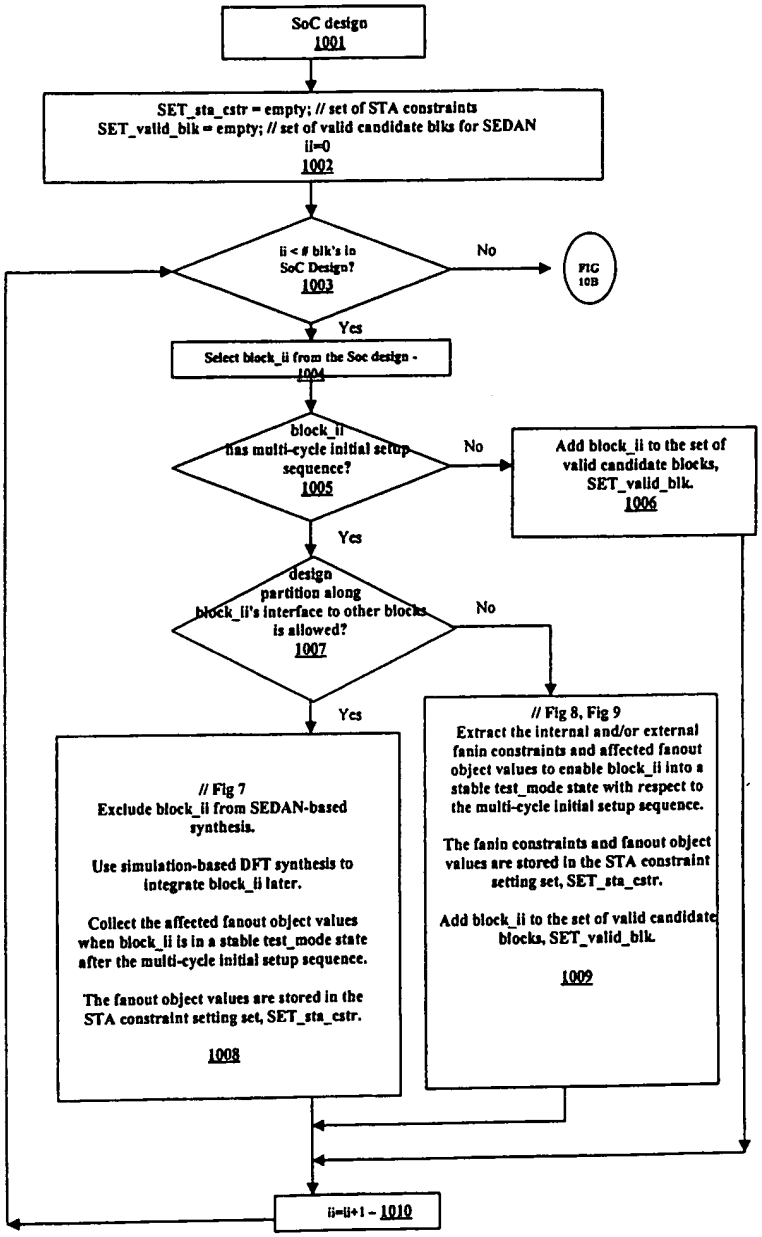

SoC design
1001
SET_sta_cstr = empty; // set of STA constraints
SET_valid_blk = empty; // set of valid candidate blks for SEDAN
ii=0
1002
ii < # blk's in SoC Design?
1003
No
FIG 10B
Yes
Select block_ii from the Soc design -
1004
block_ii has multi-cycle initial setup sequence?
1005
No
Add block_ii to the set of valid candidate blocks, SET_valid_blk.
1006
Yes
design partition along block_ii's interface to other blocks is allowed?
1007
No
Yes
// Fig 7
Exclude block_ii from SEDAN-based synthesis.
Use simulation-based DFT synthesis to integrate block_ii later.
Collect the affected fanout object values when block_ii is in a stable test_mode state after the multi-cycle initial setup sequence.
The fanout object values are stored in the STA constraint setting set, SET_sta_cstr.
1008
// Fig 8, Fig 9
Extract the internal and/or external fanin constraints and affected fanout object values to enable block_ii into a stable test_mode state with respect to the multi-cycle initial setup sequence.
The fanin constraints and fanout object values are stored in the STA constraint setting set, SET_sta_cstr.
Add block_ii to the set of valid candidate blocks, SET_valid_blk.
1009
ii=ii+1 - 1010

FIGURE 10A

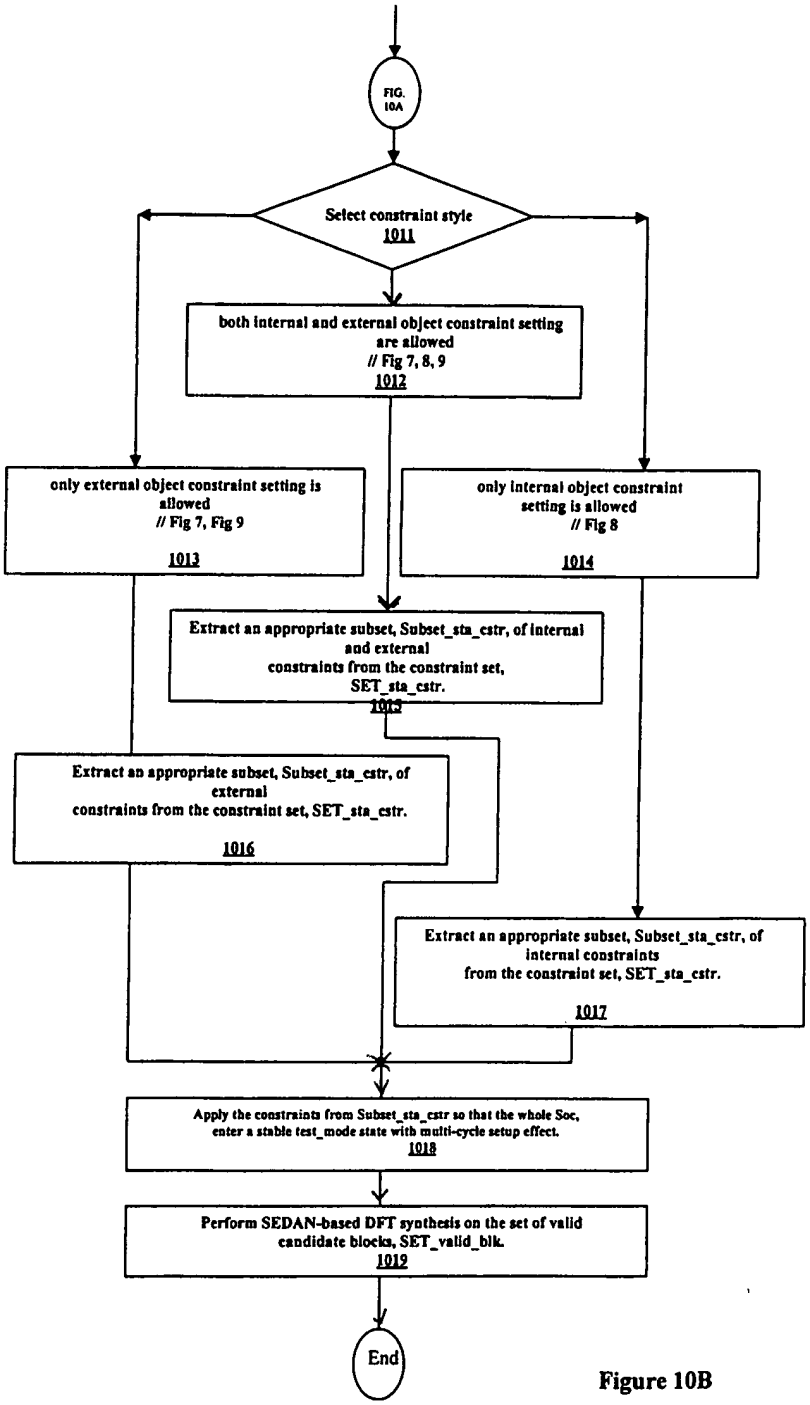


FIG. 10A
Select constraint style
1011
both internal and external object constraint setting are allowed
// Fig 7, 8, 9
1012
only external object constraint setting is allowed
// Fig 7, Fig 9
1013
only internal object constraint setting is allowed
// Fig 8
1014
Extract an appropriate subset, Subset_sta_cstr, of internal and external constraints from the constraint set, SET_sta_cstr.
1015
Extract an appropriate subset, Subset_sta_cstr, of external constraints from the constraint set, SET_sta_cstr.
1016
Extract an appropriate subset, Subset_sta_cstr, of internal constraints from the constraint set, SET_sta_cstr.
1017
Apply the constraints from Subset_sta_cstr so that the whole Soc, enter a stable test_mode state with multi-cycle setup effect.
1018
Perform SEDAN-based DFT synthesis on the set of valid candidate blocks, SET_valid_blk.
1019
End

Figure 10B

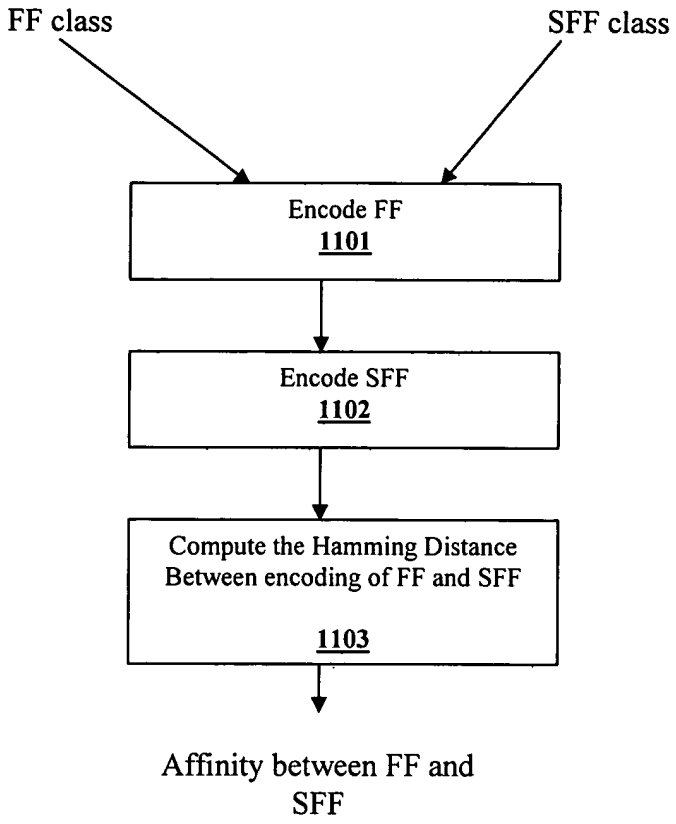

FF class
SFF class
Encode FF
1101
Encode SFF
1102
Compute the Hamming Distance
Between encoding of FF and SFF
1103
Affinity between FF and
SFF

Figure 11

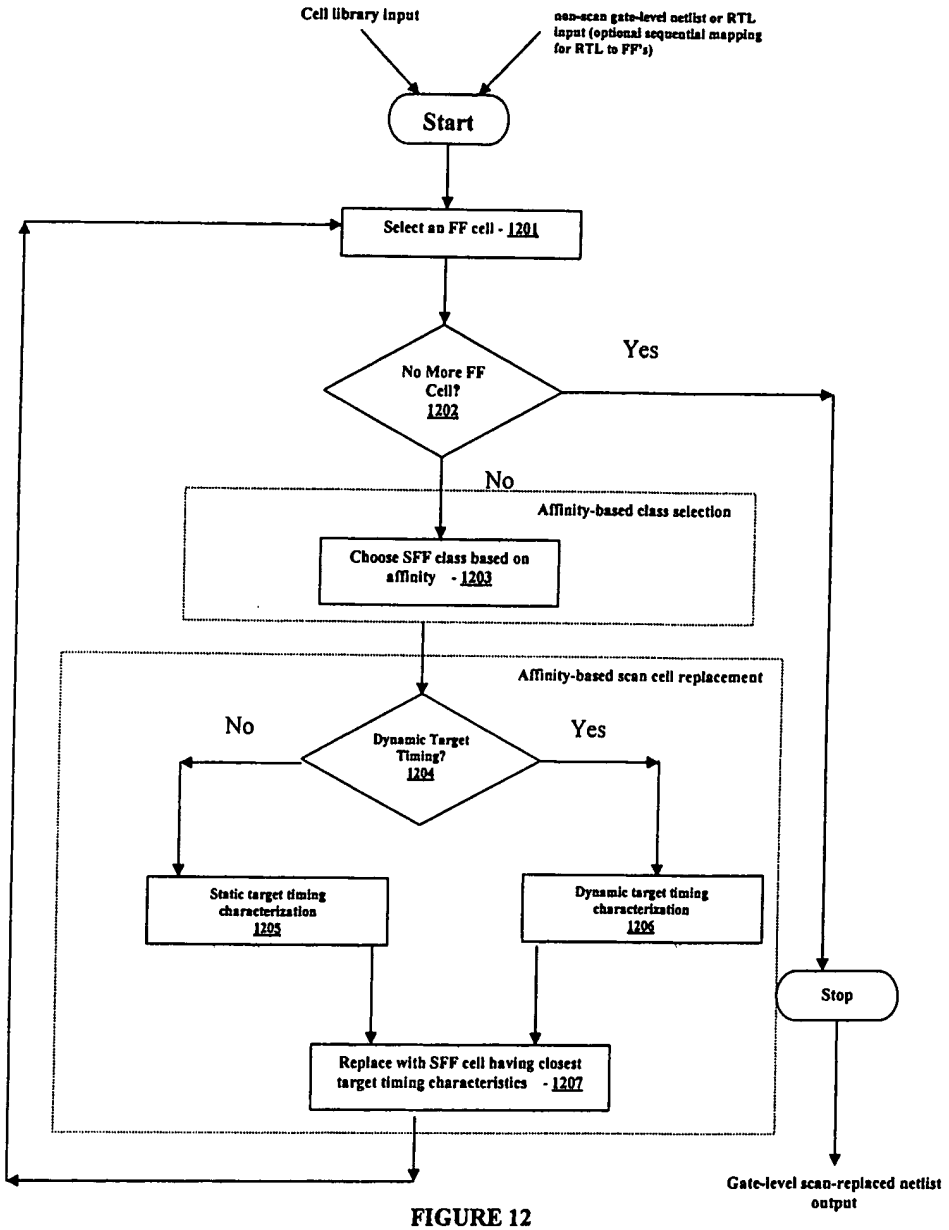

Cell library input
non-scan gate-level netlist or RTL input (optional sequential mapping for RTL to FF's)
Start
Select an FF cell - 1201
No More FF Cell? 1202
Yes
No
Affinity-based class selection
Choose SFF class based on affinity - 1203
Affinity-based scan cell replacement
No
Dynamic Target Timing? 1204
Yes
Static target timing characterization 1205
Dynamic target timing characterization 1206
Stop
Replace with SFF cell having closest target timing characteristics - 1207
Gate-level scan-replaced netlist output

FIGURE 12